Design a state machine to produce the following output waveforms. Use the standard structure that we’ve been discussing in class.

Note that Reset_N and clk are inputs to the D flip-flops, and are not needed by the logic clouds.

R is an input signal, and A and B are the output signals to be produced.

The waveforms to be produced are shown on the following page.

The definition of the circuit is as follows:

The output signals A and B follow a 5-clock sequence:

A: H H L H L
B: L H L L L

They repeat this cycle forever, except when interrupted by a Reset or the input R. When R is low, the cycle runs and repeats. When R is high, on any given clock edge, the state machine will restart its sequence on that same clock edge, beginning with the first pair of outputs listed above.